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Docket: 0756-1653

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of)
SHUNPEI YAMAZAKI et al)
Serial No. 08/818,884) Group Art Unit: 2871
Filed: 03/17/1997) Examiner: D. T. NGUYEN
For: ELECTRO-OPTICAL DEVICE AND)
METHOD FOR MANUFACTURING THE)
SAME)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 6-2-03

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner of Patents

Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

In accordance with 37 C.F.R. § 1.97(e), it is certified that either (1) each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement, or (2) no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign patent application and no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this information disclosure statement.

JP 63-208896 discloses a thin film transistor which comprises a lower gate electrode (2); a lower gate insulating film (3); a semiconductor layer for forming a

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channel (4); a pair of semiconductor layers which are doped with an impurity and function as a source and a drain (5), an upper gate insulating film (6); and an upper gate electrode (12), wherein the lower and the upper gate electrodes (2 and 12) comprises a light shielding conductive material, and wherein a lower gate wiring (2') which is an extended portion of the lower gate electrode (2) and an upper gate wiring (12') which is an extended portion of the upper gate electrode (12) are electrically connected with each other in a portion other than the thin film transistor.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,



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